

**Abstract of the Disclosure**

A delay locked loop (DLL) that applies an amount of delay to an external clock signal to generate multiple delayed signals. One of the delayed signals is selected as an internal clock signal. The multiple delayed signals have different delays in relation to the external clock signal. If a change in operating condition of the DLL occurs, such as a change in the supply voltage during an operational mode of the memory device such as an ACTIVE, a READ or a REFRESH mode, the DLL immediately selects another delayed signal among the multiple delayed signals as a new internal clock signal to compensate for the change before a phase detector of the DLL detects the change.

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